REMARKS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of applicants' certified copy of the priority document for the German Patent Application 199 17 884.4, filed April 20, 1999 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-14 are in the application.

In "Claim Rejections - 35 USC § 103" on page 2 of the above-identified Office Action, claims 1-6, 8-11, 13 and 14 have been rejected as being obvious over by U.S. Patent No. 6,311,300 to *Omura, et al.* (hereinafter **OMURA**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" on page 4 of the above-identified Office Action, claim 7 has been rejected as being obvious over **OMURA** in view of U.S. Patent No. 5,923,836 to *Barch, et al.* (hereinafter **BARCH**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" on page 5 of the above-identified Office Action, claim 12 has been rejected as being obvious over **OMURA** in view of U.S. Patent No. 5,764,655 to *Kirihata* (hereinafter **KIRIHATA**) under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a built-in self-test circuit to be connected to an external device including:

> a functional circuit connected **through an indirect interface** to a structural testing device for testing a structure of a logic circuit,
>
> the functional circuit driving the logic circuit **through a direct interface,**
>
> the functional circuit receiving test commands from an external device **through a standard interface**, and
>
> the functional circuit at least partially forwarding the test commands **to the indirect interface for indirectly driving the logic circuit.**

Independent claims 13 and 14 contain similar language. For example, Claim 14 calls for, *inter alia*, a built-in self-test circuit to be connected to an external device including:

> a logic circuit having a structure to be tested;
>
> a structural testing device for testing the structure of the logic circuit;

a functional circuit having **a standard interface** connecting the functional circuit to an external device transmitting test commands, the functional circuit receiving the test commands **through the standard interface;**

an indirect interface for indirectly driving the logic circuit, **the indirect interface connecting the functional circuit to the structural testing device;**

a direct interface connecting the functional circuit to the logic circuit, the functional circuit driving the logic circuit **through the direct interface;** and

the functional circuit at least partially forwarding the test commands **to the indirect interface.**

While the **OMURA** reference also discloses a testing apparatus for a semiconductor device, the described testing device in **OMURA** does not need to conform to "a standard interface" as recited in the claims of the instant application. As such, the **OMURA** testing device can be freely adapted to the number of pins on the integrated circuit (IC) to be tested. The number of terminals can thus be expanded for structural testing, as can be seen when comparing FIG. 1 and FIG. 6 in **OMURA.** In addition, **OMURA** allows direct access to the logical circuit through the additional pins of the IC to be tested (see *e.g.*, pin P5 and P6 in FIG. 6). As such, the scan path and any internal test points of the IC's logic units in **OMURA** can be directly and externally read and manipulated.

In contrast to the methods exhibited in **OMURA**, the instant application concerns "a chip card" as recited in claim 13 of the instant application, the chip card having a **fixed** external interface or "standard interface" having a **fixed number of external terminals** each having a defined functional allocation. In "a standard interface" one cannot add an additional terminal or interface without losing compatibility with the existing infrastructure. Moreover, the chip card described in the instant application includes secure data that must not be easily accessible through the standard interface. As such, direct structural testing must not be used, because direct structural testing would give the equivalent of direct access to the actual logic circuit, which would thereby allow for the impermissible manipulation of secure data through a direct interface.

The instant application includes "a functional circuit" that is both "driving said logic circuit through a direct interface" and "indirectly driving said logic circuit" via "an indirect interface" to a structural testing device as recited in claim 1. In this manner, direct access to the scan path and/or test points in the logic circuit from outside is impossible, while still allowing structural testing of the logic circuit through a standard interface without requiring extra terminals.

In this manner, **OMURA** is non-analogous art, because it allows and even encourages the introduction of additional infrastructure, including the use of additional interfaces and terminals, to test the semiconductor device. There is no mention of security concerns in **OMURA**, nor is there any express need for the device in **OMURA** to include an indirect interface to protect secure data on the chip card. As such, **OMURA** is silent in regards to performing structural testing using a standard immutable interface.

Clearly, **OMURA** does not show "a functional circuit" that is both "driving said logic circuit through a direct interface" and "indirectly driving said logic circuit" via "an indirect interface" to a structural testing device as recited in claim 1 of the instant application.

The **BARCH** reference discloses a computer simulation that verifies the IC design and the integrity of the serialized scan patterns that will be relied on to test fabricated ICs. **BARCH** does not show how a "functional testing device" can functionally test the logic circuit "through said direct interface" as recited in claim 6 of the instant application. Nor does **BARCH** teach or suggest using a "functional testing device" to perform "a functional test based upon a simulation

result" on both the "structural test device and said logic circuit" as recited in claim 7. In contrast, the instant application is directed towards actual testing of an IC circuit and not just a "fast, accurate, and cost effective computer simulation" to verify the IC design as indicated in **BARCH**. Verification of an IC design through simulation is used to show that if the IC is properly manufactured, the IC will operate as expected without logic errors or other preventable design related flaws, but a simulation cannot indicate the individual operability of a specific IC. Thus while a simulation is good for verifying the overall design of an IC, the only way to test the operability of a specific IC is to actually test the specific IC.

In the instant application, a built-in self-test circuit on a chip card is used to test "the structure of the logic circuit" through an indirect interface coupling a function circuit to a structural testing device.

Clearly, **BARCH** does not show a "built-in self-test circuit to be connected to an external device" as recited in claim 1 of the instant application. Nor does **BARCH** teach or suggest "a functional circuit" that is both "driving said logic circuit through a direct interface" and "indirectly driving said logic circuit" via "an indirect interface" to a structural

testing device as recited in claim 1 of the instant application. More specifically, **BARCH** does not show "said functional testing device performs a functional test" as recited in claim 7 of the instant application.

The **KIRIHATA** reference discloses a built in self test system with a self programmable non-volatile memory. The self test system provides "in the field access of chip self test results via an on chip RF transmitter" and "in the field retesting ... by providing ... on chip RF receiver for communicating a retest command." However, there is no indication in **KIRIHATA** that the on chip RF receiver and transmitter are part of the standard interface. Rather use of the RF receiver and transmitter are limited to "in the field" access and retesting.

In contrast, the built-in self-test circuit as recited in claim 12 of the instant application provides that "the standard interface is a contactless interface." As mentioned previously, the chip card contains secure data that must not be easily accessible through the standard or contactless interface. As such, direct structural testing must not be used via the contactless interface, because this type of testing would give the equivalent of direct access to the actual logic circuit, which would thereby allow for the

impermissible manipulation of secure data through a contactless interface.

Clearly, **KIRIHATA** does not show that "the standard interface is a contactless interface" as recited in claim 12 of the instant application. Nor does **KIRIHATA** teach or suggest that "a functional circuit" is both "driving said logic circuit through a direct interface" and "indirectly driving said logic circuit" via "an indirect interface" through a structural testing device as recited in claim 1 of the instant application.

Moreover, **BARCH**, **KIRIHATA**, and combinations thereof do not overcome the deficiencies of **OMURA** in the rejections of the above-identified Office Action. It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 13, and 14. Claims 1, 13, and 14 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-14 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

KHF:cgm

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